19.2 A Linear Uplink WCDMA Modulator with –156dBc/Hz Downlink SNR

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Linear modulators are usually required for spectral-efficient modulation schemes such as 8PSK or WCDMA, where the symbol constellation cannot be easily arranged to allow constant envelop transmission. Based on mixers driven by quadrature LO signals, linear modulators tend to produce relatively high noise, which is transmitted alongside the desired signal but outside its designated band. The need to safeguard the reception of other radio services, however, makes such spurious transmission highly restricted, especially in cellular standards where highly sensitive downlink (DL or RX) bands tend to be placed very close to high powered uplink (UL or TX) bands. Unless the Cartesian representation of the signal constellation is transformed into the polar form to take advantage of the low-noise characteristics of PLL-based modulators as in some EDGE implementations, a high-Q external (SAW) filter is often required to suppress out-of-band noise.

In a WCDMA transceiver, the matter is exacerbated by the wide signal bandwidth, which makes polar modulation even harder than EDGE, and full-duplex operation, where the TX noise at DL frequency affects the RX noise figure. With typical WCDMA duplexers providing around 45dB isolation, TX noise at RX frequency must be as low as –155dBc to safeguard receiver reference sensitivity. Typical modulator DL noise relative to transmitted UL signal is –145dBc. In [1], extensive effort to minimize output noise has led to a 4× improvement in SNR and 151dBc has been achieved despite a low supply voltage of 1.5V. Although it is still insufficient for dispensing the TX SAW filter from the architecture, further improvement has been found difficult and virtually all commercial WCDMA transmitters today adopt the SAW filter [2]. Because the voltage swing is severely restricted (even more so at 1.2V), increasing signal current remains the main avenue to increase SNR, but the limitations of mixer switches on linearity have made further improvement difficult. This contribution presents a technique to improve switch-transistor linearity at high currents in order to improve DL SNR to the level required for full duplex operation without TX SAW filter.

Figure 19.2.1 shows a block diagram of a typical quadrature modulator and a double-balanced mixer in its conceptual form to highlight the switching of the signal current. Minimization of noise from the switching transistors requires both their transconductance and the capacitance C at the source of each switching pair to be small. This in turn imposes limits on the size of the switch transistors such that when the baseband signal current rises towards its peak, the overlap time, in which both transistors of the switching pair are on and the output is determined more by the slope of the LO than the baseband signal, widens to the extent that linearity is no longer adequate, when the ACLR drops below acceptable levels.

To maintain linearity, it is better to stop distorted baseband current from reaching the output during the overlap time, at the expense of a slight degradation of conversion gain. Since the continuous nature of (signal) current sources makes them difficult to interrupt and switching them away poses a similar overlap problem, a single switch Q is introduced between the two switching pairs, as shown in Fig. 19.2.2, which is closed briefly each time the differential LO signals cross zero. Since the sum of the differential baseband currents is constant and each side of the differential output is connected to a pair of switching transistors driven by the same complementary LO signals, the tail current is ideally evenly and instantly split and the differential output becomes zero, as illustrated by the waveforms in Fig. 19.2.2.

When switch Q opens after the overlap period of the LO signals, the source node of the switching pair should rise to the higher LO voltage minus the V_{gs} of the conducting switching transistor, which is a function of the signal current. Capacitance C however, which has assumed a signal-independent voltage during the closing of switch Q, needs to be charged first before the signal current can be re-established in the conducting switch transistor. This presents a secondary source of nonlinearity that prevents the proposed scheme from being totally effective.

Since the largest contributor to C is the shunt capacitance C_t associated with the baseband current source, its influence can be removed by an inductor in series with the current source, as shown in Fig. 19.2.3. Acting as a current memory, the inductor maintains the signal current while absorbing the voltage change at the source of the switching pair during the closing of switch Q and isolates C_t from charge redistribution, which significantly improves achievable linearity.

The pulse signal that closes switch Q during each overlapping of the LO signals needs to be aligned with the latter as closely as possible. Figure 19.2.4 shows a possible circuit for generating such pulses by feeding a delayed-clock output back to a NAND gate. It also shows how dummy gates can be inserted into the LO paths to track the delay of the pulse-generation circuit and allow the pulse to be centred about each zero crossing of the differential LO signal.

To verify the concept and demonstrate that the TX SAW filter can be removed from a WCDMA transmitter, a full modulator test chip is realized in a 0.13μm CMOS process. The architecture is otherwise kept close to the design in [3], to better monitor the effectiveness of the proposed technique. All circuits have been redesigned for 1.2V supply, which proved to be even more challenging both for the baseband filters and the upconverting mixers, and optimized for noise performance. An external 4GHz LO signal is used but the generation of I and Q, as well as the pulsing signals are on chip. A separate 1.2V modulator circuit nearly identical to this design and without the pulsing technique is used for performance comparison.

Measurements validate both the low-noise design and the linearity improvement technique introduced above. Figure 19.2.5 shows the measured ratio between the DL noise and the modulated uplink signal power versus signal current (for one of the four branches). At 5mA the DL noise is 156dB below the carrier, making it suitable for a SAW-filter free transmitter even at a competitive 4dB overall receive noise figure. Also shown in Fig. 19.2.5 are the intermodulation products of two sine waves, which serve as a measure of achievable ACLR, versus signal current for both modulators with and without the pulsing technique. A 6dB shift in IM3 curve between the modulator with and without the pulsing technique can be observed. Twice as much signal current can therefore be sustained before linearity deteriorates. A doubling of the signal-to-noise power can therefore be achieved. There is 1dB signal loss due to reduced duty cycle, hence conversion gain. At –10dBm WCDMA modulated output the measured ACLR is –49dBc. The corresponding DL noise to carrier ratio is –156dBc, sufficient for TX SAW filter removal. A summary of the measured results is given in Fig. 19.2.6. The integrated modulator occupies 1.6×0.77mm^2. Its micrograph is shown in Fig. 19.2.7.

References:
[1] G. Brenna, D. Tschopp, and Q. Huang, "Carrier Leakage Suppression in Direct-Conversion WCDMA Transmitters," *IEEE ISSCC Dig. Tech. Papers*, pp. 270-271, Feb., 2003.
[2] D. L. Kaczman, M. Shah, N. Godambe, et al., "A Single-Chip Tri-Band (2100, 1900, 850/800 MHz) WCDMA/HSDPA Cellular Transceiver," *IEEE J. Solid-State Circuits*, vol.41, pp. 1122-1132, May, 2006.
[3] G. Brenna, D. Tschopp, J. Rogin, et al., "A 2-GHz Carrier Leakage Calibrated Direct-Conversion WCDMA Transmitter in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1253-1262, Aug., 2004.

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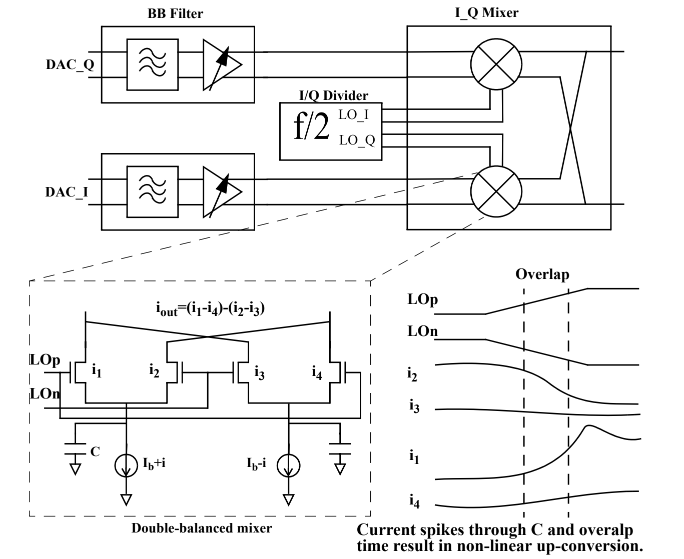

Figure 19.2.1: Modulator architecture with double-balanced mixers.

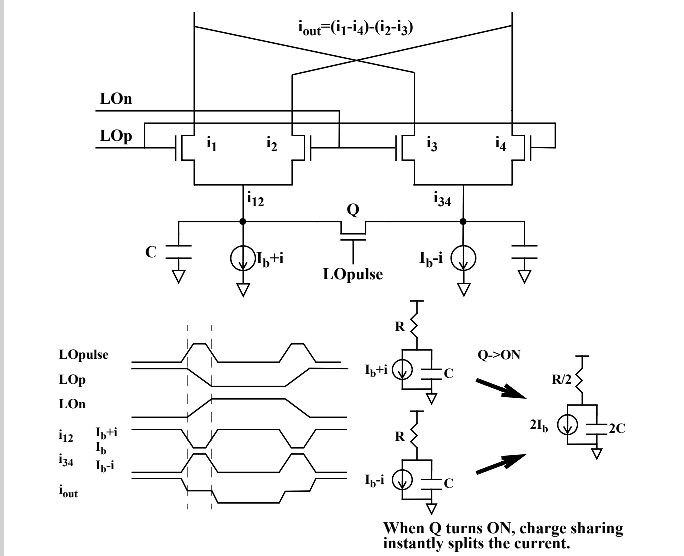

Figure 19.2.2: Quenching of overlap period.

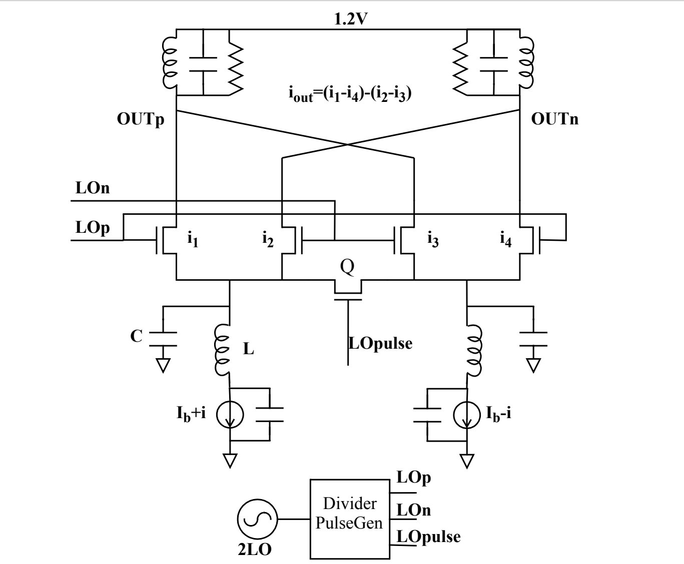

Figure 19.2.3: Mixer with quenched overlap and source inductors.

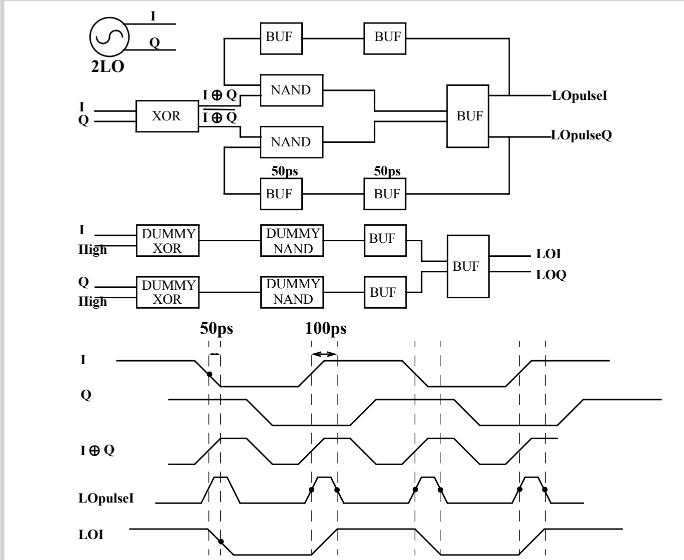

Figure 19.2.4: Quenching pulse generation.

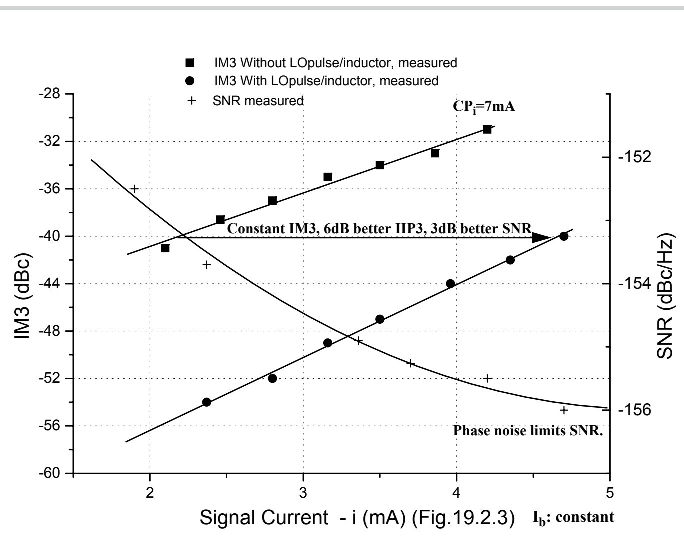

Figure 19.2.5: Measured IM3 and SNR.

Conversion gain	-5dB	WCDMA Pout	-10dBm
OIP3	+13dBm	ACLR@5MHz	-49dBc
Out-of Band Noise		ACLR@10MHz	-70dBc
@190MHz(UMTS Rx Band)	-156dBc/Hz	EVM	3%
Carrier Leakage	-45dBc		
Image Rejection	-43.5dBc		
HD3	-46.5dBc at -6.5dBm Pout		
Overall Power Consumption	113mW		
Supply Voltage	1.2V		

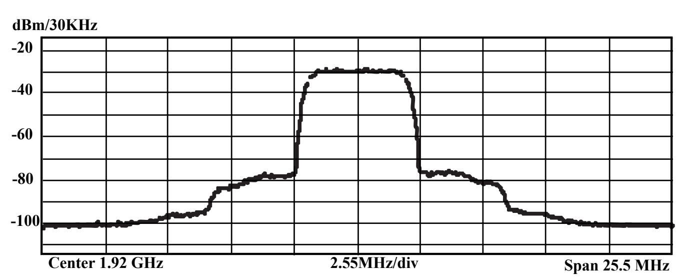

Figure 19.2.6: Performance summary and output spectrum.

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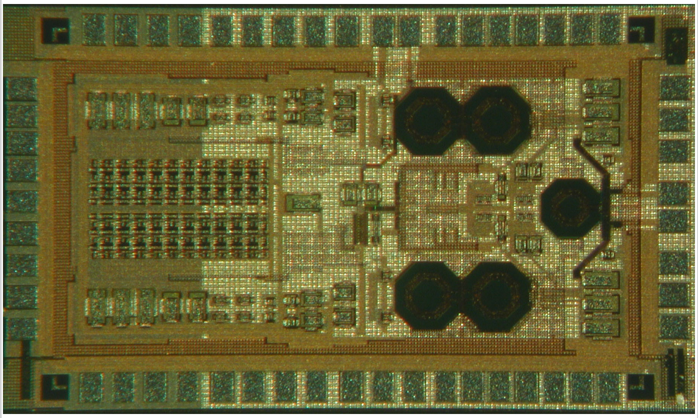

Figure 19.2.7: Chip micrograph.

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